ECE 405: Senior Design Project

NCL-Synchronous Equivalence Checker

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**Purpose:**

Our project aims to produce a tool that will prove the equivalence of synchronous digital logic circuits with an equivalent asynchronous circuit design. The purpose of this tool is to extend formal verification from previously verified synchronous circuits to an analogous asynchronous implementation of that circuit. Formal verification is the process of mathematically proving a circuit’s functionality for all inputs. This is commonly used in verifying circuit designs and ensuring the safety of digital logic circuits.

The tool automatically generates equations called Satisfiability Modulo Theorems (SMT) from a given netlist. These theorems are used to test satisfiability, which is the existence of a set of possible inputs for which the equation is true. The potential user of our algorithm must first generate a netlist for both the synchronous and asynchronous circuits. A netlist is a set of information that lists the gate type, inputs, and outputs of every gate in a digital logic circuit. The output of our tool is a file that contains two sets of expressions: a set of expressions describing the synchronous circuit, and another set of expressions for the asynchronous circuit. This file is then processed using a satisfiability solver Z3, which will verify the equivalence of the two circuit designs. Z3 will then try to find a set of inputs for which the circuits aren’t equivalent.

**Requirements**:

* Inputs: The user must provide the following inputs for both the synchronous and asynchronous circuits.
* Circuit Netlist: List of each gate’s type, bit vector size, output, and input(s).
* Circuit Inputs List: List of every input in the circuit. There must be a list for the synchronous and asynchronous, as well as a general inputs list for both, which is used for matching purposes and determining equivalence.
* Circuit Outputs List: A list of every output in the circuit. This is used for matching the outputs of the synchronous and asynchronous circuits.
* Functionality
* Output